SONY

CXD1267AN

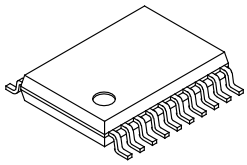
CCD Vertical Clock Driver

Description

The CXD1267AN is a vertical clock driver for CCD image sensors. This IC is the successor of the CXD1250N with attractive features.

Power consumption is reduced approximately 30% for the CXD1267AN version.

20 pin SSOP (Plastic)



Features

1) Substrate voltage (Vsub) generator is built-in.
   - Variable Vsub in the range of 4.0V to 18.5V.
   - Reduction of peripheral parts saves space.
2) Only two power supplies (+15V and –8.5V) are needed.
3) 3.3V clock interface is acceptable.
4) 20-pin SSOP package is used.
5) Low power consumption
   90mW (CXD1267N)
   62mW (CXD1267AN)
   approximately 30% reduction

Appllications

CCD cameras

Structure

CMOS

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_L	0 to –10	V
• Supply voltage	V_H	V_L – 0.3 to 2V_L + 35	V
• Supply voltage	V_M	V_L – 0.3 to 3.0	V
• Input voltage	V_I	V_L – 0.3 to V_H + 0.3	V
• Output voltage (V2, V4)	MVϕ	V_L – 0.3 to V_M + 0.3	V
• Output voltage (V1, V3)	HVϕ	V_L – 0.3 to V_H + 0.3	V
• Output voltage (VSHT)	HHVϕ	V_L – 0.3 to V_H + 0.3	V
• Operational amplifier output current	I_{DCOUT}	±5	mA
• Operating temperature	Topr	–25 to +85	°C
• Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_H	14.5 to 15.5	V
• Supply voltage	V_M	0	V
• Supply voltage	V_L	–6.0 to –9.0	V
• Input voltage (except for pin 3)	V_I	0 to 6.0	V
• Operational amplifier input voltage	V_{IOP}	1.0 to 4.5	V
• Operating temperature	Topr	–20 to +75	°C

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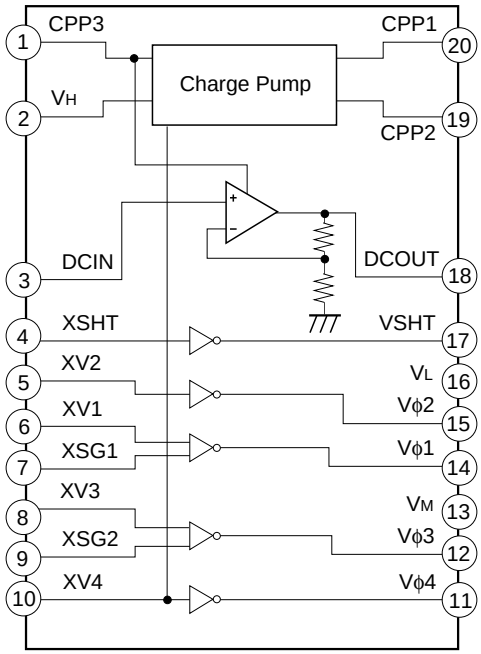
Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	CPP3	O	Charge pump
2	V_H	—	Power supply (15V)
3	DCIN	I	Operational amplifier input
4	XSHT	I	Output control (VSHT)
5	XV2	I	Output control (Vϕ2)
6	XV1	I	Output control (Vϕ1)
7	XSG1	I	Output control (Vϕ1)
8	XV3	I	Output control (Vϕ3)
9	XSG2	I	Output control (Vϕ3)
10	XV4	I	Output control (Vϕ4)
11	Vϕ4	O	High-voltage output (2 levels: V_M, V_L)
12	Vϕ3	O	High-voltage output (3 levels: V_H, V_M, V_L)
13	V_M	—	GND
14	Vϕ1	O	High-voltage output (3 levels: V_H, V_M, V_L)
15	Vϕ2	O	High-voltage output (2 levels: V_M, V_L)
16	V_L	—	Power supply (–8.5V)
17	VSHT	O	High-voltage output (2 levels: V_H, V_L)
18	DCOUT	O	Operational amplifier output
19	CPP2	—	Charge pump
20	CPP1	—	Charge pump

Truth Table

Input				Output		
XV1, 3	XSG1, 2	XV2, 4	XSHT	Vφ1, 3	Vφ2, 4	VSHT
L	L	X	X	V_H	X	X
H	L	X	X	Z	X	X
L	H	X	X	V_M	X	X
H	H	X	X	V_L	X	X
X	X	L	X	X	V_M	X
X	X	H	X	X	V_L	X
X	X	X	L	X	X	V_H
X	X	X	H	X	X	V_L

X: Don't care
Z: High impedance

Electrical Characteristics

DC Characteristics (Unless otherwise specified, Ta = 25°C, V_H = 15V, V_M = GND, V_L = –8.5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.3	—	—	V
Low level input voltage	V_{IL}		—	—	1.3	V
High level output voltage	V_{OH}	I_O = –20µA	14.9	15.0	—	V
Middle level output voltage	V_{OM1}	I_O = 20µA	—	0.0	0.1	V
Middle level output voltage	V_{OM2}	I_O = –20µA	–0.1	0.0	—	V
Low level output voltage	V_{OL}	I_O = 20µA	—	–8.5	–8.4	V
Charge pump output voltage	V_{CPP3}	–1 ≤ I_{CPP3} ≤ 0mA I_{DCOUT} = 0mA, Ta = –20 to 75°C V_{IOP} = 4.5V	20	—	—	V
Input current	I_I	V_I = V_L to 5V	–1.0	0.0	1.0	µA
Operating supply current	I_H	*1	—	1.4	2.0	mA
Operating supply current	I_L	*1	–6.0	–5.0	—	mA
Output current	I_{OL}	Vφ1 to 4 = –8.0V	25	—	—	mA
Output current	I_{OM1}	Vφ1 to 4 = –0.5V	—	—	–10	mA
Output current	I_{OM2}	Vφ1, 3 = 0.5V	9	—	—	mA
Output current	I_{OH}	Vφ1, 3 = 14.5V	—	—	–12	mA
Output current	I_{OSL}	VSHT = –8.0V	12	—	—	mA
Output current	I_{OSH}	VSHT = 14.5V	—	—	–7	mA
Operational amplifier gain	G	I_{DCOUT} = –200/+100µA	—	× 4.40	—	
Gain error	ΔG	Ta = –20 to 75°C*2 I_{DCOUT} = –200/+100µA V_{IOP} = 1.0 to 4.5V	–3	—	+3	%

*1 See Measurement Circuit. Shutter speed: 1/10000.

*2 See Operational Amplifier Gain Characteristic.

Note) Current directions: + indicates the direction flowing to IC; – indicates the direction flowing from IC

Switching Characteristics (V_H = 15V, V_M = GND, V_L = –8.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLM}	*1	30	50	75	ns
Propagation delay time	T_{PMH}	*1	30	50	75	ns
Propagation delay time	T_{PLH}	*1	30	50	75	ns
Propagation delay time	T_{PML}	*1	50	80	120	ns
Propagation delay time	T_{PHM}	*1	50	80	120	ns
Propagation delay time	T_{PHL}	*1	50	80	120	ns
Rise time	T_{TLM}	$V_L \rightarrow V_M$ *1	360	600	900	ns
Rise time	T_{TMH}	$V_M \rightarrow V_H$ *1	330	550	770	ns
Rise time	T_{TLH}	$V_L \rightarrow V_H$ *1	30	50	75	ns
Fall time	T_{TML}	$V_M \rightarrow V_L$ *1	180	300	500	ns
Fall time	T_{THM}	$V_H \rightarrow V_M$ *1	330	550	770	ns
Fall time	T_{THL}	$V_H \rightarrow V_L$ *1	24	40	60	ns
Charge pump boosting time	T_C	*2	—	—	10	ms
Output noise voltage	V_{CLH}	*3	—	—	0.5	V
Output noise voltage	V_{CLL}	*3	—	—	0.5	V
Output noise voltage	V_{CMH}	*3	—	—	0.5	V
Output noise voltage	V_{CML}	*3	—	—	0.5	V

*1 See Response of Voltage Pulse.

*2 CP1 = 0.1µF, CP2 = 0.1µF, V_{CPP3} = 20V; boosting time after all power supplies rose.

*3 See Noise on a Waveform.

Note) Each item is evaluated by Measurement Circuit.

Notes on Operation (See Application Circuit.)

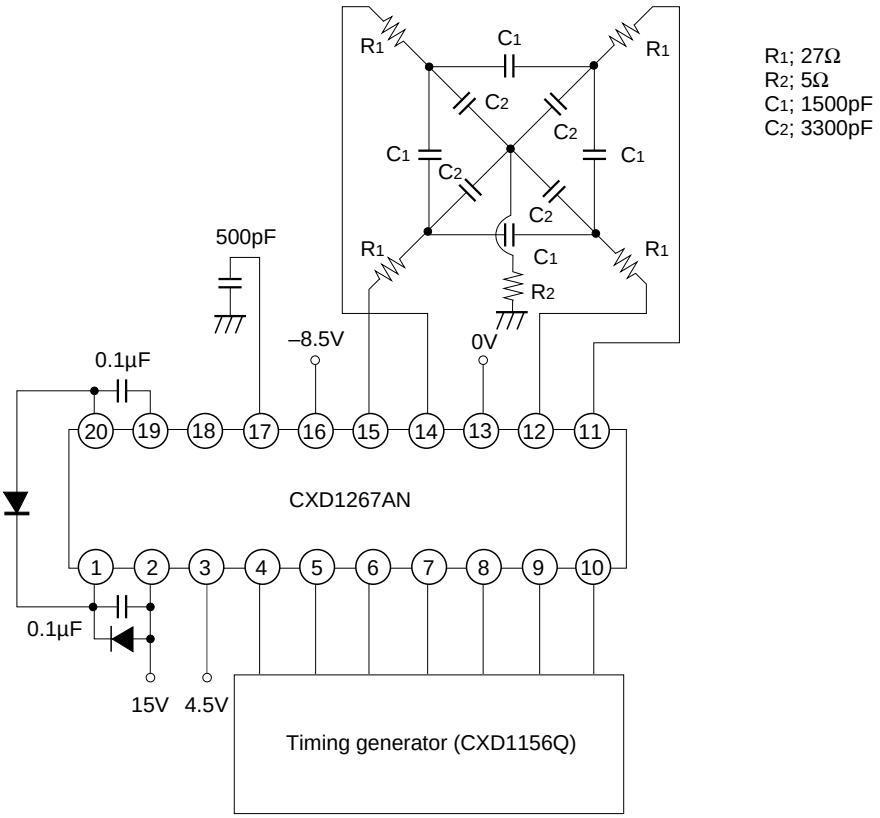
1. Be sure to protect against static electricity because this IC is MOS structure.

2. A bypass capacitor is connected between each power supply (V_H, V_L) and GND.

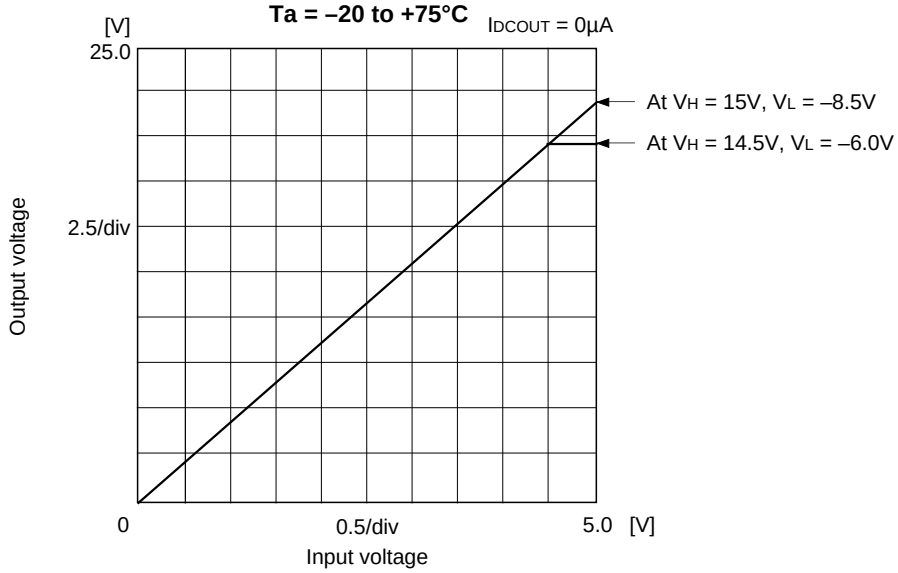
3. To prevent latch-up, use a capacitor of 0.1µF (CP1, CP2) for charge pump.
   Insert a silicon diode (D2) between CPP3 and CPP1.

4. In order to protect CCD image sensor, pre-clamp is requested prior to clamp by DCOUT.

Measurement Circuit



Operational Amplifier Gain Characteristics

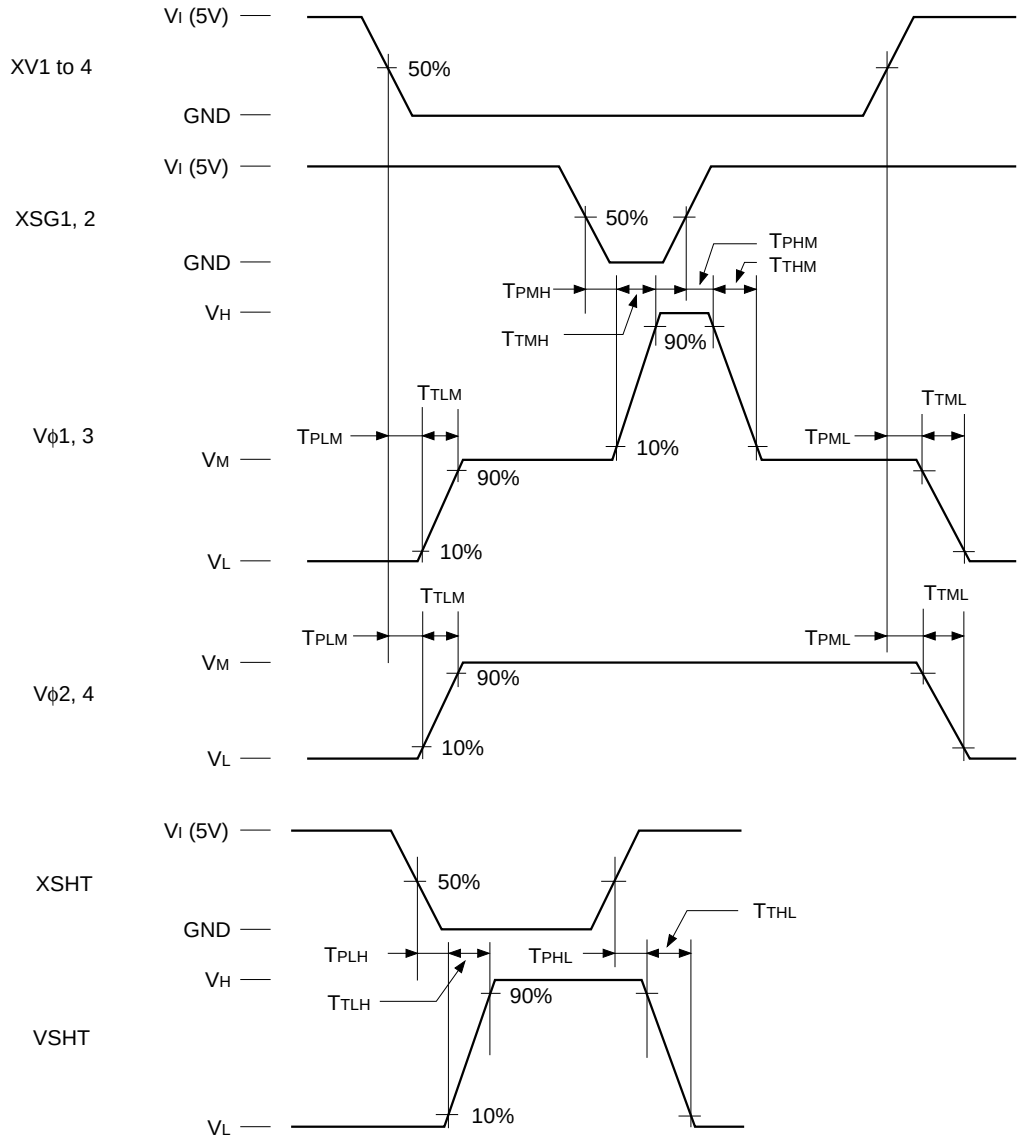


Note) Operating amplifier maximum output voltage is restricted as shown in the formula below depending on supply voltage setting of V_H and V_L.

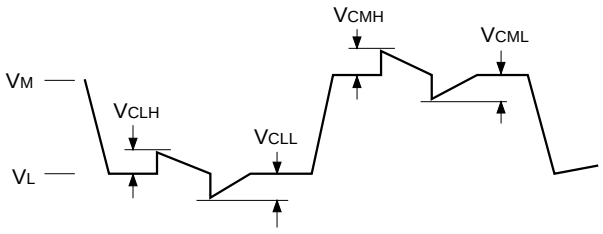
Maximum output voltage V_{DCOUT} (max) ≈ V_H + | V_L | – 0.8V

For instance, when V_H = 14.5V and V_L = –6.0V, output voltage is saturated at approximately 19.7V as shown above figure.

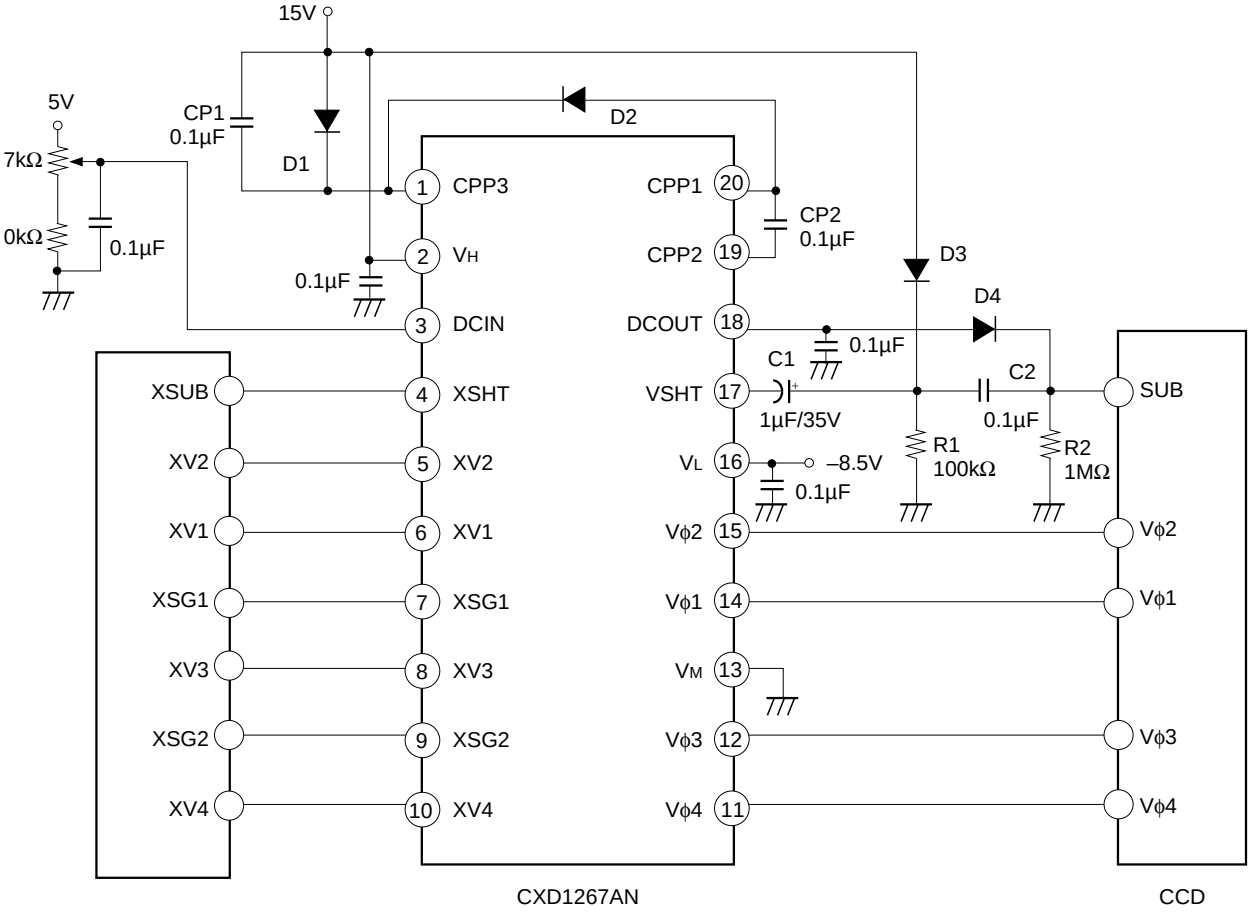
Response of Voltage Pulse



Noise on a Waveform



Application Circuit

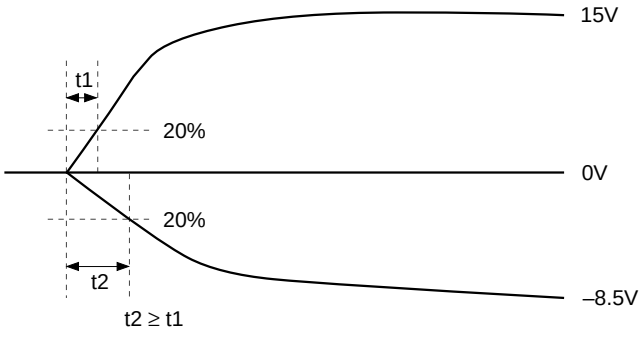


* A peripheral circuit can be simplified by CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

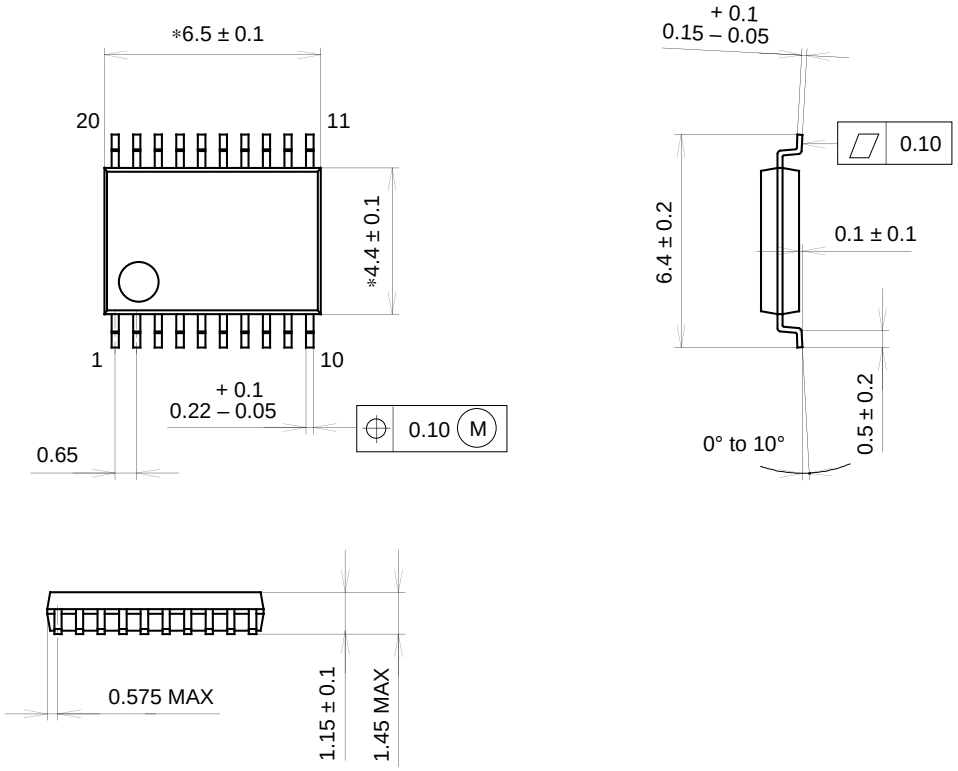
Note with power-on sequence

To protect CCD image sensor, rise two power supplies as follows.



Package Outline Unit: mm

20PIN SSOP (Plastic)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L071
EIAJ CODE	SSOP020-P-0044-AN
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	Cu ALLOY
PACKAGE WEIGHT	0.1g